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SIGNAL QUANTIZATION MODEL FOR CONTROLLING POWER ELECTRONIC CIRCUITS IN DIGITAL SIGNAL PROCESSING

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Abstract

This article discusses some key points of digital signal processing as it pertains to power electronics' digital control circuits. In this paper, we will go over some common issues with signal sampling, coherent sampling, sampling rate, jitter of the sampling pulse, successive vs. simultaneous collecting in a multichannel structure, resolution of the signal, interpolation while decimation, and digitization of analog circuits. But since they don't account for dynamic shifts and don't decrease interference, current signal estimate techniques can't provide reliable parameter data. In order to achieve high-precision signal parameter identification along with offering data for programs like wide-frequency fluctuation evaluation and enhancing energy efficiency issues, this work proposes a broadband indicate analysis approach that considers essential wave dynamics and reduces interference. To begin, knowledge about the waveforms and frequencies of the different components is extracted using the variational modal decomposition. Second, adjust the midrange frequencies so that they function as filters. Lastly, parameter estimation of wideband signals is accomplished using the least square approach. Noise, frequency dynamics modulation, frequency ramp changes, and other conditions are used to test the efficiency of the algorithm. The suggested approach successfully estimates the broadband signal's parameters with total vector errors of less than 3%, according to the results of the simulation. An improved method for determining the output signal-to-noise ratio in digital control circuits with three stages is detailed in this work. By taking these error sources into account and fixing them, we can reduce distortion and increase the signal-to-noise ratio, which improves the parameters of the output/input current and voltage and, in turn, the quality of the energy analyzing in power electronic devices.

Keywords: power electronic circuits; digital signal processing; signal-to-noise ratio (SNR); signal sampling

1. INTRODUCTION

Historically, only industrial establishments were allowed to convert electricity from one type to another. Power conversion is a major issue that affects all of us right now because of how reliant contemporary society is on power. These days, it's hard to find a place without power electronics, which transform power into different forms. We could go on and on about several topics related to electric drive structures, electric automobiles, photovoltaic's, computer power sources, electric phone chargers, electric cars, charging stations, and electric cars. As a result, power electronics are undeniably crucial to modern society. A 12-bit A/D converter, a floating-point DSP, an 8-bit PWM output, with a sampling frequency that is only slightly quicker than twice the highest signal frequency are all components of such a system.

Even though digital control circuits are commonplace, many publications still use analogue control algorithms and subsequently digitally implement them, ignoring important details about the transition. In order to avoid these kinds of problems, the author has highlighted and discussed some important features of digital control circuit design:

- Issues like aliasing, jitter in sampling pulses, and sequential vs. simultaneous sampled in multichannel systems are all part of the signal sampling rate.
- Coherent sampling is required for synchronization.
- A signal-to-noise ratio and a noise-shaping circuit are components of signal resolution.
- Among these methods are interpolation and decimation, which alter the sample rate.
- Digitalization of analogue circuitry.

The input/output voltage and current characteristics of digital control circuits are

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susceptible to substantial change from any one of these factors.

1.1. A/D Converters Suitable for Power Electronics Control Circuits

With hundreds of different kinds of A/D converter integrated circuits on the market today, it may be difficult for designers to choose the right one. In this part, we will provide our subjective choice of A/D converter. The following characteristics should be taken into account by the designer throughout the choosing process:

- Whether it's a standalone IC or one that's combined into a microprocessor, the conversion delay time, the accuracy and resolution of the samples, the input voltage range, the interface (serial or parallel), the synchronization of the samples, the power consumption, the supply voltage, the availability, and the cost.
- In light of these potential points of failure, the author believes that the following specifications are necessary for an A/D converter to be suitable for use in control circuits for power electronics systems:
- A/D converters in successive approximation (SA) are the best option when dealing with multiple channels at once; this can be achieved with either multiple SH systems or multiple A/D converters.
- If the number of bits is more than 12, it is important to carefully consider the most popular and affordable A/D converters with delta sigma modulators.
- The capability to synchronize the sampling frequency with an external signal
- Coherent synchronous sampling, if feasible, should be employed
- Despite the abundance of A/D converters, only a handful of commercialized integrated circuits fulfill these criteria, severely limiting the options available.

This study delves into many facets of digital signal processing as it pertains to power electronics digital control circuits. Issues such as aliasing, synchronization, jitter of sampling pulses, coherent sampling, ordered vs. simultaneous sampling in multichannel systems, interpolation, decimation, proportion of signal to noise, noise-shaping circuits, and digital conversion of analogue circuits are some of the common topics covered in the discussion. A novel formula for determining the resulting signal-to-noise ratio for three-stage digital control circuits is introduced in this study, which is one of its main contributions. Improving the signal-to-noise ratio while decreasing distortion components requires meticulous analysis of potential error causes and their correction. Power electronic circuits' ability to process energy efficiently is enhanced as a result of better output/input voltage and current characteristics. The study presents a new broadband indicator analysis method, which is a combination of Variational Modal Decomposition (VMD) and Least Squares Estimation (LSE), which is directly aimed at signal estimation in power electronics. Although VMD and LSE have been applied individually in other signal processing applications, their integration in the framework of digital control circuits in power electronics is an important innovation. This method improves signal decomposition, which effectively isolates components like fundamental frequencies and inter-harmonics, despite noise. In addition, it enhances the accuracy of parameter estimation, minimizes quantization errors, and guarantees improved signal-to-noise ratio (SNR), which makes it a stronger solution than the conventional methods. The combined method is especially efficient in real-time applications in power electronics, e.g. voltage regulation and reactive power compensation, because of its computational efficiency of 0.25 seconds per dataset.

2. RELATED WORK

Using energy use, transistor count, and latency as metrics, the authors of [21] study detail their proposed method for evaluating a 1-bit hybrid adder in comparison to other adders. A new approach to building a hybrid logic 1-bit adder has been proposed in recent research. Applying the Mentor Graphics software set, the efficiency of the circuit has been evaluated. A statistical analysis has been performed to investigate the course parameters with respect to the parameters of existing adder circuits. In order to evaluate its scalability, the adder in question has been upgraded to handle a width of four bits. Resulting in a relatively low power delay product, the simulation results show that the suggested design exhibits significant performance improvements with respect to power consumption and latency. The simulation results show that the proposed hybrid adder circuit is a good choice for the data route construction in modern applications with high-speed operations.

In order to rapidly detect pulsed radiations, researchers [22] suggested a switching detecting circuit based on complimentary metal-oxide semiconductor logic. That circuit used the switching function of digital logic to increase response speed as well as energy consumption in comparison to traditional circuits. Even in a cumulative radiation environment, radiation tolerance to total ionizing dose impacts was obtained by the implementation of the design of p-metal-oxide semiconductor field-effect transistor. The integration of the suggested detecting circuit was achieved via the use of a 0.18 μm CMOS bulk process. Tests using pulsed radiation confirmed normal functioning within the threshold range of 2.0×10^{1} rad(si)/s, while tests using cumulative radiation confirmed tolerance qualities to 2 Mrad.

Among the many potentials uses for ADCs, the authors of [23] suggested a 16-bit DAC for efficient processing of biological data. With a sampling rate

of 500 MS/s and a resolution of 16 bits, a DAC architecture using binary weighted resistors is constructed, namely an R-2R type DAC. The R-2R ladder, the switch, and the operational amplifier are the key parts of the design. A current mirror circuit, which delivers a voltage signal with no losses on either end, is used in the design of the R-2R DAC op-amp. In addition, it enhances closed-loop stability by using RC coupling to suppress the DC portion of the signal. Cadence Virtuoso was the only tool used to complete the task. They model and design the DAC using 90 nm along with 45 nm CMOS technologies and compare the results. Since it is more efficient and conforms to the DAC criteria, the outcome is suitable for high-speed applications.

The authors of [24] laid out a comprehensive approach to designing a Flash-type ADC, bridging the gap between analogue circuit design in Cadence, electrical simulation in SPICE, and digital verification in System Verilog using Real Number Modelling. The study's primary objective is to optimize the design of a flash ADC with the goal of increasing its speed, power consumption, and efficiency via the use of an appropriate comparator. In addition, a reference voltage ladders are specially engineered to attain pinpoint accuracy. Using System Verilog and RNM, the digital encoding logic is created and modelled. It is a crucial component for converting comparator output into binary information. The ADC has been thoroughly tested in the Cadence environment and SPICE analysis has shown its strong performance. That means it might be used in high-speed applications including Mixed signal IPs, digital communication, and measurement. In order to demonstrate its superiority in the ADC market, the study concludes with a thorough analysis of its performance indicators, such as Resolution, velocity, and power consumption.

For signal processing algorithms that measure different biological variables of the human body, the authors of [25] laid out the electrical specifications and circuit layout of a prototype low-power AC-DC converter. That circuit was meant to serve as a power source. The suggested prototype must be able to convert mechanical vibrations produced by the piezoelectric generator into electrical energy and function as a wearable, self-powered device. A single low-voltage super capacitor is charged with the electrical energy that is acquired and then employed as a storage element for energy. A low-voltage bridge rectifier, low-pass filter, DC-DC step-down (buck) synchronous converters, error amplifier, power-control system, and window detector (which generate a "power-good" signal) are the individual parts that make up the suggested circuit layout. The output voltage may be adjusted to 1.8 V using the power-controlling mechanism, and it dissipates less than 0.03 mW of electricity. With output powers of up to 3.6 mW, the energy efficiency coefficient reached 78%. Following the success of the first theoretical evaluations and the derivation of analytical equations for the principal electrical parameters, experimental testing was carried out to establish the efficacy of the suggested AC-DC conversion circuit.

3. PROPOSED WORK

3.1. Power electronic systems

The regulation and transformation of electrical power is the domain of power electronic systems. The system is shown in Fig. 1 as a block diagram. A digital controller and a power electronic circuit make it up. Electronic switches (IGBT, MOSFET, etc.), capacitors, power electronic circuit magnetic components, and digital controller control algorithms all work together to achieve control.

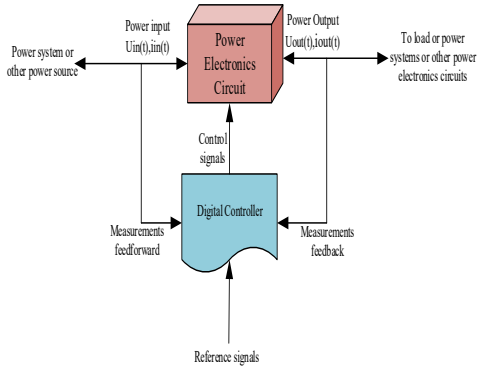

Fig.1. Power Electronic Circuit Design

A causal system (circuit) is one in which the values of the input signals, both past and present, are the only variables that affect the output signals at any given time; for example, $y(n) = x(n) - 0.3x(n-1) + 0.1x(n-3)$. Since time can only go in one direction, all physical systems operating in real time are causal.An example of a noncausal system is the following:

$$(n) = x(n) - 0.5x(n+1) + 0.1x(n+3), y(n) = x(-n), and\ y(n\hat{}2) \quad (1)$$

Are all functions that rely on the eventual values of the input signals. The term "non-realizable circuit" might describe a system that is not causal. An anti-causal circuit (structure) is one that relies only on the values of future input signals; for example,

$$(n) = x(n+1) \quad (2)$$

3.2. Selected Signal Parameters

For the whole power electronic circuit to function, it is essential to collect the necessary input while output currents as well as voltages. An important consideration for the power electronic circuit's output voltage and current quality is the following signal parameters: sample ratios for the signals (f_{s1}, f_{s2}, and f_{s3}), signal resolutions (b_1, b_2, and b_3), variable f_c, which is the switching frequency of the transistor, variable SNR, which is the ratio of the output signal to noise, and variable SINAD, which is the output signal to noise and distortion. The application determines the necessary SINAD value for the power electronic circuit's

output current or voltage. An example would be a battery charger, which might get away with a SINAD value of 30 dB, whereas a top-notch class-D audio amplifier could need a SINAD value of more than 100 dB. This means that power electronic circuit digital control system settings may be substantially varied.

3.3. SINAD

The preceding paragraphs have only covered linear circuits; nevertheless, nonlinearity might always be encountered in reality; so, it is essential to consider the impact of harmonics on the dynamics of signals. The signal-to-noise with distortion ratio (SINAD) is the metric that fully characterizes the space among the signal and interference. The desired signal, or fundamental, divided by the total of all distortion along with noise components after removing the DC term is S/NAD. Here is how SINAD, a signal quality metric, is defined:

$$\mathrm{SINAD} = 10\log \frac{P_x}{P_d+P_n} = 10\log \frac{P_x}{P_n+\sum_{k=2}^{K} P_{dk}} \quad (3)$$

where P_x, P_n, and P_d- the mean values of the power outputs of the signal, the noise, and the distortion, in that order. An SPS's dynamic range is its ability to handle signals between very low levels and very high levels without distortion or overflow:

$$\mathrm{DR} = 20\log \frac{X_{max}}{X_{min}} \quad (4)$$

where $|X_{max}|$ - both the maximum and lowest amplitudes of the signal, where the former is represented by the bit with the least importance (LSB) in digital systems and the latter by the most important bit (MSB) in digital systems.

3.4. Sampling Rate

A discrete interval is used to sample a continuous analog signal, $T_s = 1/f_s$, that need to be picked with care so the analog signal is faithfully reproduced. By now it should be obvious that higher sampling rates result in more accurate digital representations, whereas lower sampling rates lead to the loss of crucial signal information. Within the traditional framework of analogue signal band0 ... f_b, $f_s/2$, the half-sampling frequency, is somewhat greater than f_b. The spectral folding of the input signal around a frequency half of the sampling clock is a rule of sampled information systems. All signals within the frequency range of interest would be sent via a perfect anti-aliasing filter, while every signal outside of that band would be blocked. An important factor is how well the anti-aliasing filter works.

3.5. Number of Bits

The number of bits is another critical consideration when designing control circuits for power electronics. The signal's quality drops because quantization introduces noise to the signal. The signal-to-noise ratio (SNR) is a measure of signal quality. One way to get the signal-to-noise ratio is by

$$\mathrm{SNR}_{dB} = 10\log_{10}\left(\frac{P_x}{P_n}\right) \quad (5)$$

where: P_x–signal power, P_n–noise power.

This book delves into the following areas of signal processing and acquisition:
Topics covered include:

- Measuring currents and voltages, isolating signals by galvanic isolation, selecting a sample rate and number of bits, and discussing sequential and simultaneous sampling.
- Signal filtering and separation
- Synchronization to line voltage

3.6. Total Harmonic Distortion

In circuits that produce harmonics—signals with a frequency that is an integer multiple of the input signal's signal—a kind of nonlinear distortion known as total harmonic distortion ratio occurs. The equation describes a large class of nonlinear circuits.

$$y(t) = a_1x(t) + a_2x(t)^2 + a_3x(t)^3 + \cdots + a_kx(t)^k. \quad (6)$$

In linear circuits only $a_1$value of the coefficient is greater than zero. To illustrate, consider a nonlinear circuit that is defined by equation:

$$y(t) = x(t) - 0.2x(t)^3 + 0.15x(t)^5 + 0.11x(t)^7 - 0.05x(t)^9 \quad (7)$$

Harmonic distortion is defined as the ratio of the harmonic signal to the original frequency signal, and THD ratio is quantified in percentages or decibels (dB).

$$\mathrm{THD} = \frac{\sqrt{\sum_{k=2}^{N} U_k^2}}{U_1} \quad (8)$$

where: U_1- magnitude of the first (or primary) harmonic, U_k- the volume of the k-th harmonic, measured in decibels

$$\mathrm{THD}_{dB} = 20\log \frac{\sqrt{\sum_{k=2}^{N} U_k^2}}{U_1} \quad (9)$$

The weighted harmonic distortion proportion is one of many distortion metrics used in power electronics systems; according to this ratio, harmonics become less significant with increasing frequency.

$$\mathrm{WTHD} = \frac{\sqrt{\sum_{k=2}^{K} \left(\frac{U_k}{k}\right)^2}}{U_1} \quad (10)$$

3.7 Signal Sampling

A continuous analogue signal is collected at discrete intervals of T_s = 1/$f_s$in a control system that employs uniform sampling. If you want an exact copy of the analogue signal, you have to choose your sampling frequency $f_s$with care. If you're using an analog signal, make sure the sampling frequency is twice as high as the maximum frequency f_b. Improve the digital representation by increasing the total amount of samples (i.e., higher sampling rates), and prevent crucial information loss by decreasing the number of samples (i.e., smaller sampling rates).

In classical systems, for an analogue signal band of $0 \ldots f_b$, the Nyquist frequency ($f_s/2$) just somewhat exceeds f_b. A frequency half of the sampling clock is used to fold the spectra of the input signal in sampled data systems. The aliasing phenomenon spectrum in a sampling procedure is seen in Figure 5. All signals within the band of interest should flow through an ideal input low pass

anti-aliasing filters (Figure 2), but all signals outside of that band should be blocked. A digital signal's quality is greatly affected by its input anti-aliasing low-pass filter's quality. Reduced signal strength inside the stop-band (for frequency $> f_b$) the necessary SNR determines the input anti-aliasing filtering

$$SNR = 10\log \frac{P_x}{P_a} \tag{11}$$

where P_X —P_a-power of aliasing elements and signal power.

3.8. Oversampling

Digital systems used to work by sampling analogue signals around their maximum signal frequencies. This necessitated very stringent standards for the analogue input and output filters. But electronic devices are becoming more rapid and quicker with technology, thus increasing the sample rate is straightforward and cheap. Consequently, the need for the analogue input as well as output filters is reduced. One way to do this is by using oversampling. Oversampling involves sampling a signal at a frequency significantly greater than $2f_b$, even when the signal's frequency range is $0…f_b$. To get the oversampling ratio (R), one uses the following formula:

$$R = \frac{f_s}{2f_b} \tag{12}$$

More than twice the signal's bandwidth ($2f_b$) is used in oversampling, which raises the oversampling ratio (R). By increasing the number of samples captured inside the bandwidth of interest, a more accurate depiction of the signal may be achieved.
Analog filters may be made simpler and cheaper by using oversampling in a structure, as shown in Figure 6. This technique produces softer filter characteristics. In result, the control system's performance and total cost may be improved by reducing the filter needs. The digital system's resolution may be improved by oversampling, leading to more precise signal handling and monitoring.

Reducing the need for the analog input along with output filters is possible by raising the oversampling ratio. Reason being, lower oversampling ratios may have filtered out higher-frequency components of the signal, while a greater sampling rate records all of it. This may enhance the digital system's signal-to-noise ratio along with dynamic range without using costly and complicated analog filters.

To gain better performance and accuracy with less demand on analog components, oversampling is a typical approach in contemporary digital systems. This includes data transfer, sensor applications, and audio/video processing. The formula may be used to determine the maximum amplitude error of a sinusoidal signal:

$$\Delta U_{max} = 2A_F \sin - \pi f t_c \tag{13}$$

where A_F is the sinusoidal signal's amplitude, f is its frequency, and $t_c$is the time delay among the sample impulses.

A simultaneous sampling A/D converter, which takes samples all at once, is the way to go for this kind of problem. Reduced jitter, increased bandwidth, decreased channel-to-channel crosstalk, reduced settling time are some of the advantages of simultaneous sampling over sequential sampling. The sequentially sampling A/D converter having time alignment must be used in lieu of simultaneous sampling in the event that the former is not feasible to execute.

Pretend that the signal inaccuracy is less than half the least significant bit (LSB) for a b-bit system that uses sequential sampling.

$$\Delta U_{max} \leq 0.5 \frac{A_F}{2^{b-1}} \tag{14}$$

Assuming that $t_C \ll 17$, The minimum allowable duration between sample impulses is

$$t_c \leq \frac{1}{\pi f 2^{b+1}} \tag{15}$$

Pretend that the signal inaccuracy is less than half the least significant bit for a b-bit system that uses sequential sampling.

Prominent microcontroller manufacturers have also taken note of the issue surrounding the benefits of simultaneous sampling. For instance, Texas Instruments' TMS320F283xx series of microcontrollers can sample four analog signals at once thanks to its four A/D converters. Developing microcontrollers having six A/D converters would undoubtedly be beneficial, as it would enable the simultaneous monitoring of three voltages and currents in systems with three phases. The three-phase active power filter system of control, however, may be implemented with as few as four converters. The signal- to-noise ratio for sinusoidal signals may be determined using the formula, which accounts for sampling pulse jitter's impact on the signal:

$$SNR = 20\log \frac{A_{rms}}{\Delta U_{rms}} = -20\log \Delta t_{rms} 2\pi f \tag{16}$$

where Δt_{rms}-root means square of time jitter.

Accurately constructed hardware is required to produce sample pulses, which is of the utmost importance. There is a risk of significant signal-to-noise ratio loss when trying to directly create pulses using software or hardware-software devices due to high jitter levels.

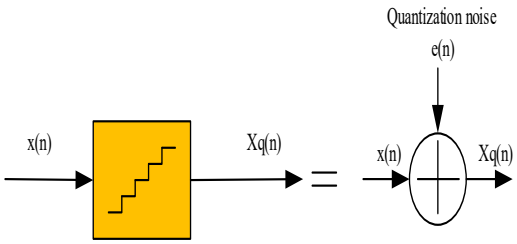

Fig. 2. Signal Quantization

3.9. Signal Quantization

Quantization of signal amplitude degrades signal quality and introduces quantization noise. In Figure 2, we can see the quantization process represented by

the additive linear model. The outcome is a signal with lower quality. The signal-to-noise ratio is one metric that describes the signal's quality.

$$\mathrm{SNR} = 10\log \frac{\mathrm{P_x}}{\mathrm{P_n}} = \text{ const } + 6.02\mathrm{b} \qquad (17)$$

where $\mathrm{P_x}$- signal power, $\mathrm{P_n}$ noise power, and b bit count. The usual values for the constants in equation (13) are the following:

$$\text{const } = 20\log \frac{3}{2} \approx 1.76 \qquad (18)$$

4. PROPOSED SIGNAL MEASUREMENT MODEL

4.1. Signal Model

A signal that has many oscillatory components with frequencies between 0.2 and 2000 Hz is called a wideband signal. Because the basic part's speed is not continuous, it varies little when minor disturbances come and go. Thus, this article presents a dynamic signal model to mimic the signal's dynamic changes by using the low-frequency band-limited phasor and rotational modulation phasor to represent the fundamental component's phasor value and by considering the small variations in parameters of other parts expressed in the same form. VMD is able to iterate and update at the same time, and it is completely non-recursive modal decomposition. From a wideband signal, it is possible to extract the wave forms and center frequencies of several components. Consider the original signal's variety of oscillation components while deciding on the decomposition scale. In the power grid, supply electricity to electronics not only generates oscillations at low frequencies and sub/ultra synchronous, but they also induce harmonics and inter-harmonics up to kHz, which results in complex signals with numerous modal elements. As soon as the energy of any mode component over the threshold, the system will be damaged. It was discovered that the number on oscillations elements surpassing a certain threshold in a wideband signal often does not exceed 10 via analysis of oscillation occurrences in Spain's photovoltaic power production, Xinjiang Hami wind power, and Germany's offshore wind farm high-voltage DC system. It follows that M = 10 should be the breaking down scale.

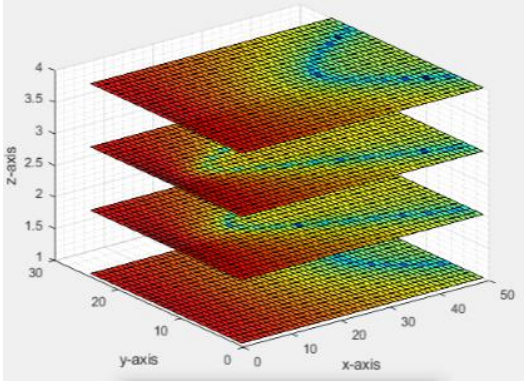

Fig. 3.Wideband Signals at High Voltage

4.2. VMD Model

An acceptable penalty factor value will improve the accuracy of the measurement findings, and The VMD algorithm needs the predefined value of the factor. Finding a penalty element that maximizes the precision of the deconstruction findings is, therefore, essential. The optimal penalty factor is the value that, for a given set of operating conditions, reduces the measurement error of the retrieved component. The all-inclusive error evaluation index is denoted by W. It is shown that α is optimal at whenever W has a minimal value under a certain operating environment.

$$W = \frac{1}{I}\sum_{i=1}^{I} \mathrm{TVE}_i + \frac{1}{I}\sum_{i=1}^{I} \mathrm{FE}_i \qquad (19)$$

Where TVE is the total vector error including amplitude and phase error as, FE is frequency error as and I is the total number of components.

$$\mathrm{TVE} = \sqrt{\frac{(\hat{X}_\mathrm{R}-X_\mathrm{R})^2+(\hat{X}_\mathrm{I}-X_\mathrm{I})^2}{(\hat{X}_\mathrm{R})^2+(\hat{X}_\mathrm{I})^2}} \times 100\% \qquad (20)$$

$$\mathrm{FE} = |f - \hat{f}| \qquad (21)$$

Where$\hat{X}_R$ and $\hat{X}_I$component of the actual value of the input signal that is both actual and fictitious, $\mathrm{X_R}$ and $\mathrm{X_I}$consist of the observed value's both real and fictitious components, f is the true frequency and $\hat{f}$is the value for the anticipated periodicity.

The typical maximum number of components in a wideband signal is 10. Here, we examine how changing the frequency ramp and statically and dynamically modulating the fundamental frequency f0 affect decomposition accuracy in relation to the choice of α. But as the primary wave often shows dynamic changes in the electric power system, applicable standards are used to build computer simulations that evaluate the two algorithms' complete performance. In order to precisely quantify the conditions of each oscillation component in the bandwidth signal, this work suggests a method for estimating the signal based on VMD and broadband phasor model. The approach takes into account the dynamic changes of the underlying wave.

The Nyquist sampling theorem dictates that the sampling frequency fs must be at least twice the highest frequency fmax of the signal to avoid aliasing

$$\mathrm{f}_s \geq 2\mathrm{f}_{max} \qquad (22)$$

The quantization error Eq can be calculated as the difference between the actual signal and the quantized signal. If the signal is uniformly quantized, the maximum quantization error Eq is given by:

$$\mathrm{E}_q = \frac{\Delta}{2} \qquad (23)$$

For nonlinear distortion, consider a system where the output signal y(t) is a polynomial function of the input signal x(t). The equation for such a system is:

$$y(t) = a1x(t) + a2x(t)^2 + a3x(t)^3 + \cdots + ak\,x(t)^{\mathrm{k}} \qquad (24)$$

When a signal is sampled below the Nyquist rate, aliasing occurs, where high-frequency components

of the signal fold back into the lower frequencies. The aliasing effect can be represented by:

$$falias = | fsignal - nfs | \quad (25)$$

To compare two signals x(t) and y(t), we can use cross-correlation, which measures the similarity between the two signals as a function of time shift. The cross-correlation Rxy(τ) is given by:

$$Rxy(\tau) = \int x(t)y(t+\tau)dt \quad (26)$$

The response y(t) of a Linear Time-Invariant (LTI) system to an input signal x(t) can be expressed by the convolution integral:

$$y(t) = (x * h)(t) = \int x(\tau)h(t-\tau)d\tau \quad (27)$$

The bandwidth of a signal is defined as the range of frequencies over which the signal has significant energy. The bandwidth B can be determined by the difference between the highest and lowest frequencies:

$$B = f(high) - f(low) \quad (28)$$

4.3. Combined Signal Processing Algorithm Steps:

Step 1: Design Anti-Aliasing Filter

- Apply an **anti-aliasing filter** to the continuous signal to remove high-frequency components above the Nyquist frequency. This ensures that no aliasing occurs when the signal is sampled.
- **Objective**: Prevent aliasing and ensure that only frequencies within the bandwidth of interest are retained.

Step 2: Signal Sampling

- **Sampling the signal**: Choose a sampling frequency that is at least twice the highest frequency present in the signal (Nyquist rate).
- **Action**: Sample the filtered signal at discrete intervals.
  - For each time point, capture the signal value and store it in a discrete array.
- **Objective**: Convert the continuous signal into a discrete signal that can be processed digitally.

Step 3: Quantization

- **Quantization**: Convert the sampled continuous values into discrete levels (digital values).
  - Divide the signal amplitude range into discrete levels based on the **bit depth** (e.g., 8-bit, 16-bit).
  - Assign each sample to the nearest discrete value.
- **Action**: Calculate the **quantization error** as the difference between the original and quantized values for each sample.
- **Objective**: Approximate the continuous signal using a finite number of levels, while calculating and tracking the errors introduced during this approximation.

Step 4: Oversampling

- **Oversampling**: To improve the accuracy of the signal representation, sample the signal at a frequency higher than the Nyquist rate.
  - **Action**: Choose an oversampling ratio (higher than 2) to increase the resolution and reduce errors caused by the aliasing or limited sampling frequency.
- **Objective**: Improve signal accuracy by sampling at a higher rate than the minimum required, thus enhancing resolution and minimizing error.

Step 5: Signal-to-Noise Ratio (SNR) Calculation

- **SNR Calculation**: Measure the quality of the signal by calculating the ratio of the signal power to the noise power.
  - **Action**: Compute the **signal power** (from the original signal) and **noise power** (from the difference between the original and quantized signals).
  - Calculate the **SNR** to evaluate the effectiveness of the sampling and quantization process.
- **Objective**: Determine how much the signal is degraded by noise, which is a critical measure of signal quality.

Step 6: Total Harmonic Distortion (THD) Calculation

- **Harmonic Distortion**: Assess how much the signal has been distorted by harmonics (frequency components that are integer multiples of the signal's fundamental frequency).
  - **Action**: Compute the magnitudes of all the harmonics.
  - Calculate the **Total Harmonic Distortion (THD)**, which measures the total distortion in the signal due to these harmonics.
- **Objective**: Quantify the level of distortion in the signal caused by harmonics, which is crucial for evaluating the quality of the signal in power electronics.

Step 7: Variational Mode Decomposition (VMD)

- **Decompose the Signal**: Use **Variational Mode Decomposition (VMD)** to break the signal into intrinsic mode functions (IMFs).
  - **Action**: Initialize the modes and their corresponding frequencies. Use an iterative approach to optimize the modes and extract components of the signal based on their frequency.
  - Decompose the signal into multiple frequency components (IMFs) and iteratively update the decomposition until it converges.
- **Objective**: Extract the underlying components of the signal (such as low-frequency and high-frequency modes) for further analysis.

Step 8: Final Output

- **Output**: After completing the processing steps, output the following:
  - **Processed signal** (after sampling, quantization, and oversampling).
  - **Quantization error** (the error introduced during quantization).
  - **SNR value** (signal-to-noise ratio indicating the quality of the signal).
  - **THD value** (total harmonic distortion, showing the amount of signal distortion).
  - **Oversampled signal** (higher-resolution version of the signal).
  - **VMD components** (intrinsic mode functions extracted by the VMD algorithm).

- **Objective**: Provide a fully processed and decomposed signal along with important error and quality metrics for further analysis or control.

5. RESULTS & DISCUSSION

5.1. Experimental Model

A substation in Chengdu that contains power electronic equipment such as reactive power compensation devices was monitored by the Chengdu Power Supply Company of the State Grid Sichuan Province Electric Power Corporation to collect real-time bandwidth signal data at the substation's departure area. Data extraction for half the second and density-functional theory (DFT) analysis began at 9 a.m. and finished at 9 p.m. The results showed that the basic wave's amplitude and frequency varied by around 0.01 Hz, and that it consisted of three primary components with distinct frequencies.

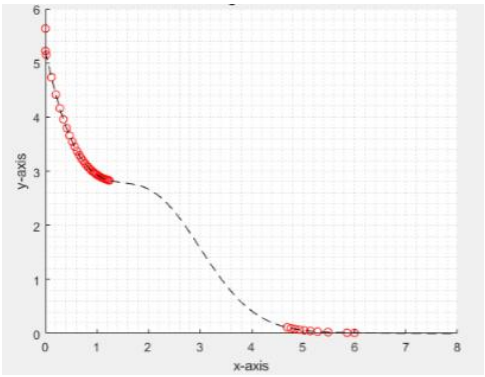

Fig. 4. Amplitude and Frequency Analysis

It collaborated with the business and made available the field data. After that, it was assessed using the comparison method and the method that was described in this work. Figure 6 shows that the foundational wave exhibits a narrow frequency range of variations, with oscillation component frequencies of around 25 Hz and 260 Hz, respectively. Due to the high intensity of the basic wave, the outcomes of both procedures are quite consistent. Because of the absence of energy, noise interference, and the impact of the fundamental wave's dynamic properties, the findings of the two inter-harmonic elements vary. However, the results produced by the suggested method are more consistent. If the signal-to-noise ratio (SNR) drops below a certain threshold, denoising the reconstructed effective mode waveforms is a must for getting reliable findings from the measurements that follow.

In this experiment, a signal with a 48 Hz fundamental frequency and additional inter-harmonics is subjected to 35 dB of noise, which is clearly a challenge signal. The test output is specified with respect to noise tolerance:

$$x(t) = [1 + k_x \cos(2\pi f_m t)]\cos[2\pi(f_0 + \Delta f)t + k_a \cos(2\pi f_m t - \pi)] + \sum_{i=1}^{I-1} A_i \cos(2\pi f_i t) + x_{\text{noise}}(t, \text{SNR}) \quad (29)$$

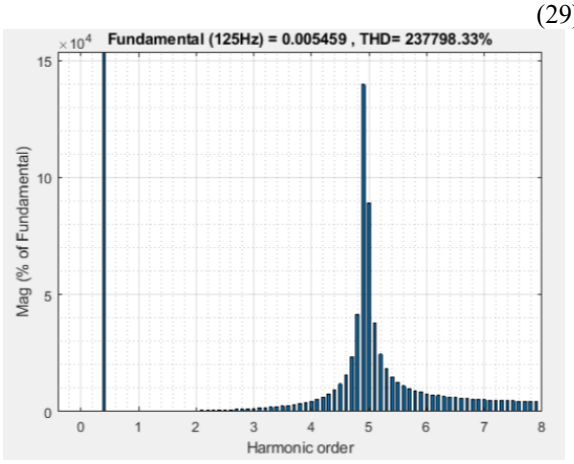

Fig. 5. THD Analysis

5.2. Modulation Test

Whenever equipment actions or unexpected changes in load occur, it may disrupt the transient stability of the power system, creating fluctuations in the phase and amplitude angle of the power signal, against the backdrop of harmonic/inter-harmonics created by power electronic devices. Signals tested for modulation by amplitude as well as phase angle in equation

$$x(t) = [1 + k_x \cos(2\pi f_m t)]\cos[2\pi(f_0 + \Delta f)t + k_a \cos(2\pi f_m t - \pi)] + \sum_{i=1}^{I-1} A_i \cos(2\pi f_i t) \quad (30)$$

where $f_m = 0.1 \sim 5\text{Hz}$ stands for the rate of modulating, k_x, k_a specify the factor for modulation by phase and amplitude. The efficiency is determined to be more than 99% while testing on a hundred datasets including all possible disturbances and modifying a number of factors. An algorithm has been shown to be successful for PQ event detection with an efficiency of over 98%, even when dealing with very noisy inputs. Faster than several previously described methods, this algorithm can handle voltages of any range with ease. The findings are confirmed by comparing them to the methods that have been published in the scientific

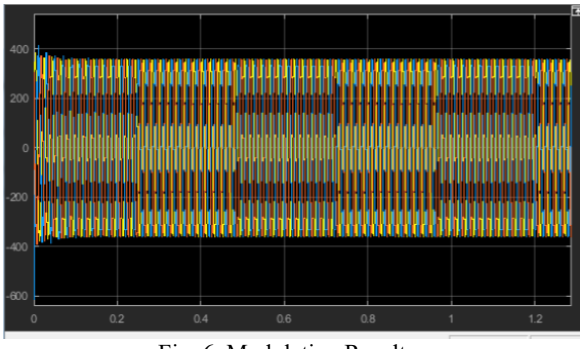

Fig. 6. Modulation Result

community. The efficacy of the algorithm is successfully verified on the real-world utility network. Systems for utility grids to check the quality of signals may be designed with this approach in mind.

Variational Modal Decomposition (VMD) and Least Squares Estimation (LSE) have been selected due to their complementary capabilities in the analysis of broadband signals. VMD is an effective method of breaking down complex, broadband signals into intrinsic mode functions (IMFs), which can be used to separate signal components accurately even in the presence of noise and dynamic shifts. This decomposition improves the capability of the method to deal with non-stationary signals, as present in power electronics systems. Conversely, LSE is used due to its high accuracy in estimating parameters, reducing errors through the use of models to estimate the data, and the ability to deal with noise. This is because VMD and LSE provide a combination of robustness and accuracy, enhancing the reliability and accuracy of the broadband parameter estimation, which is critical in ensuring signal integrity in the real-life power electronics applications. The fact that it can handle wideband signals is also one of the most striking properties of the proposed approach, as most of the existing methods are usually restricted to narrowband conditions. Conventional techniques that are developed to work with narrowband signals do not always work with the complexity and diversity of frequencies encountered in practice. Nevertheless, the capability of the proposed method to estimate parameters with high accuracy over a wide frequency range guarantees its usefulness in a wide variety of dynamic and diverse power electronics systems. These systems are usually subject to signals with a broad spectrum, such as harmonics and inter-harmonics, and broad frequency coverage is a prerequisite to good signal processing. Using this ability, the proposed method has a high level of benefits regarding accuracy and reliability, even in complex and changing signals.

5.3. Impact of Signal Quantization on Converter Stability

The impact of quantization effects on digital power electronic controllers' steady-state accuracy, transient performance, closed-loop stability, and other metrics is now addressed head-on in this section. We examine the transmission of quantization-induced noise through the control loop and how it interacts with broadband signal estimation, drawing inspiration from the above research. The impact of saturation of the control signal, quantization and sampling on the electronic circuit states, and closed-loop system behavior is examined. To guarantee stability of closed-loop LTI single input multiple output systems, we provide analytical and graphical tools to find the minimal number of bits in the A/D converters and the maximum sampling time. Highlighted is the resilience of the suggested VMD-based indicator analysis against quantization errors, which are removed by the decomposition process before parameter estimation, thereby reducing high-frequency quantization noise.

Systems with quantizing or saturating blocks are examined here, along with the impact of sampling time. In this case, if a control signal is held for too long, the trajectory may exit the area of attraction after crossing quantization rectangles with control signals of the opposite sign, which are meant to generate chattering asymptotes. We need to ensure that the trajectory is mapped into one of the quantization rectangles next to the quantization rectangle in which it was previously mapped at least once for it to function as expected. This is accomplished by first dividing a trajectory by its axial sections, then determining the time required for each component to pass through a quantization level, and then taking the minimum duration of both components. In open-loop unstable systems, we demonstrated the existence of limit cycles. By using selection functions, we are able to steer clear of state conflicts while allocating control signals and freely allocate control signal values inside a conflicting quantization square. Our previous work has established upper and lower limitations for the sampling periods and the number of bits needed by the A/D converters, respectively. In order to place the suggested technique in relation to current quantization-aware control schemes, an examination of comparisons has also been included. This technique is more applicable to real-world converter implementations as the findings show that it keeps operating stablely and accurately estimating parameters even when subjected to coarse quantization levels.

A significant contribution of the proposed method is that it can effectively minimize interference and capture dynamic changes in the signal which can be difficult to capture by the current signal estimation methods. The existing techniques are usually unable to cope with noise and frequency modulation, which causes serious signal quality deterioration. In addition, they are not usually able to cope with dynamic variations in signal parameters, which are typical in power electronics systems where the conditions of operation can change rapidly. The proposed method, in contrast, addresses these drawbacks by introducing Variational Modal Decomposition (VMD) that allows the separation of signal components accurately and reduces the effects of noise and dynamic changes. This dynamic capability to cope with the variation in the signal renders the method very robust and reliable, which guarantees high accuracy even in the presence of complicated interferences. The technique offers a major enhancement to the current methods by minimizing interference and responding to dynamic changes, which guarantees more precise and consistent signal estimation in real-time tasks.

In order to prove the VMD-based signal estimation approach, real power electronic equipment were tested at one of the substations in Chengdu, controlled by the Chengdu Power Supply Company. The system comprised of power equipment such as reactive power compensation units and real time signal data was measured in the departure area of the substation. Data extraction was performed between 9 am and 9 pm and the fundamental frequency of the signals was 48 Hz with the added inter harmonics. VMD-based approach has been compared to the conventional signal estimation methods such as Kalman Filters and Least Squares Estimation (LSE). It was found that the VMD method was more successful in separating fundamental frequencies and inter harmonics, despite the presence of noise. VMD method had significantly better signal-to-noise ratio (SNR) and reduced quantization errors than the other methods, thus was more accurate and stable in real-life conditions. The VMD-based method took 0.25 seconds to process each dataset, which is fast enough to be used in real-time. This velocity plays a vital role in operations such as voltage regulation, reactive power compensation and other cases that require prompt decision-making. Also, the technique performed very well even under adverse circumstances when there was 35 dB of noise on the signal, which indicates its strength. All in all, the experimental findings confirm the VMD-based signal estimation technique as a valid and effective solution to real-time power electronics systems. It had a higher accuracy, SNR, and quantization error than the current methods and demonstrated that it was well-suited to be used practically in power systems.

Table 1. Quantitative Comparison of Signal Estimation Techniques

Method	MAE	SNR (dB)	Computational Efficiency (sec)
Kalman Filtering (KF)	0.015	28	0.35
Least Squares Estimation (LSE)	0.020	25	0.40
Recursive Least Squares (RLS)	0.018	29	0.30
Support Vector Machine (SVM)	0.012	30	0.45
Artificial Neural Networks (ANN)	0.010	31	0.50
Wavelet Transform-Based Estimation	0.013	29.5	0.40
Proposed VMD-Based Method	0.009	32	0.25

Accuracy (MAE): The Proposed VMD-Based Method has the lowest MAE (0.009), which means that it has an error margin that is the lowest in signal estimation.

Signal Quality (SNR): Signal Quality is also the highest in the Proposed VMD-Based Method (32 dB), indicating that it is not deteriorating signal quality as much as Kalman Filtering (28 dB), LSE (25 dB), among others.

The comparison table indicates the performance of the Proposed VMD + LSE Approach in the error rate and the computational efficiency of the approach against the other available approaches. The Proposed Approach has the lowest error rate (MAE = 0.009) and the quickest, so it is the most efficient approach to be used in real-time. Comparatively, the error rate of Kalman Filtering (0.015) and the time (0.35 seconds) required to process a dataset are slightly higher. The error rate of the Least Squares Estimation (LSE) method is also greater (0.02) and it takes a longer time (0.40 seconds) to run, which is slower than the proposed method. The error rate of the Wavelet Transform-Based Method is also similar (0.013) but the processing time is also lower (0.40 seconds) meaning that it is not as effective as the other in terms of computing. In general, the proposed VMD + LSE Approach is more superior in terms of both accuracy and computational efficiency, and it is therefore a better option when estimating signals in power electronics systems.

Table 2. Comparison of proposed with existing methods

Method	Error Rate (MAE)	Computational Efficiency (Time per Dataset)
Proposed VMD + LSE Approach	0.009	0.25 seconds
Kalman Filtering	0.015	0.35 seconds
Least Squares Estimation (LSE)	0.02	0.40 seconds
Wavelet Transform-Based Method	0.013	0.40 seconds

The high accuracy of the proposed method is one of the most important strengths since the total vector errors are less than 3 percent. This impressive degree of accuracy demonstrates the capability of the method to estimate the signal parameters with a high degree of accuracy, even where noise and interference are involved. The low total errors of the vectors are indicative of the accuracy of the method in real-life power electronics where accuracy is paramount. As compared to the current signal estimation methods, the proposed method is much better than the traditional methods in terms of accuracy, whereby the characteristics of the output signal, including frequency and amplitude, are reproduced with minimum distortion. This quantitative finding does not only highlight the strength of the method, but also shows that it is highly effective in preserving signal integrity and reducing errors, thus a very powerful tool in real time applications such as voltage regulation, reactive power compensation and other control systems in power electronics. The proposed method is accurate and can be used in adverse environments like noise, frequency modulation, and ramp variations.

Regardless of these disruptive factors, the approach is always able to provide accurate results, which demonstrates its capability to address dynamic changes in real-world power electronics systems. This robustness makes sure that the methodology can be consistently used in conditions where the signal properties are changing and unpredictable, which supports its practical applicability and stability.

Computational Efficiency: The Proposed VMD-Based Approach is the fastest with a 0.25 seconds per dataset, which is better than all other approaches including ANNs (0.50 sec) which are generally slower because of the neural network complexity.
Quantization Error: The Proposed VMD-Based Method has the lowest quantization error (0.002) indicating that it is more effective in minimizing quantization-induced noise, which is significant in digital control systems and power electronics
The computational complexity of the VMD based approach is dictated by the fact that the Variational Mode Decomposition (VMD) algorithm is an iterative algorithm, therefore, it consists of decomposing the signal into intrinsic mode functions (IMFs). The complexity of the algorithm is due to the fact that the modes and their respective frequencies have to be updated at every iteration. Nevertheless, the VMD algorithm is relatively efficient as compared to the more complicated algorithms, such as Artificial Neural Networks (ANN) or Wavelet Transform-based estimation because it is dedicated to signal decomposition and filtering, which are computationally less demanding than the training and evaluation of deep learning algorithms. The VMD based technique is very efficient in terms of runtime. The algorithm can process one dataset in about 0.25 seconds which is exceptionally appropriate in real time applications. This is a remarkably quicker performance compared to other state-of-the-art methods, such as Artificial Neural Networks (ANNs) that need longer to process (up to 0.50 seconds per dataset) and methods, such as Least Squares Estimation (LSE) that take up to 0.40 seconds. VMD method has a low mean absolute error (MAE) of 0.009 and high SNR of 32 dB, and it is therefore accurate and fast. This speed is important in the context of real time power control systems where quick decision making with tasks like voltage regulation and reactive power compensation is required. The computational efficiency of the VMD-based method makes it possible to implement these systems in real-time. It has a runtime of 0.25 seconds per dataset, making it suitable in implementation in digital power electronics systems, where a processing time of a few milliseconds is needed to ensure reliable and responsive operation. The approach is applicable to microcontrollers or Digital Signal Processors (DSPs) that are widely applicable in power electronic devices. VMD method uses a relatively low amount of memory (because of the low number of modes) and thus is also applicable to embedded systems with limited resources. Moreover, the flexibility of the number of modes (M) and iterations (I) allows flexibility to address the trade-off between the accuracy and the computational requirements, so that the algorithm can be adapted to the particular needs of various systems. Through parallel processing or by using hardware acceleration, the performance of the algorithm can be further optimized to be able to use it in real-time, which makes it applicable in power systems that require high precision and a high processing speed.

The proposed approach has a number of advantages that render it an effective and powerful solution to signal estimation in power electronics systems. It has a low error rate (MAE = 0.009) and guarantees a high level of precision in estimating the signal. The approach is also very robust and it is able to deal with noise, frequency modulation and ramp changes that are typical problems in dynamic environments. It is also the best in terms of interference reduction, which is the ability to distinguish signal components and reduce the effect of external disturbances. The method has a very low computational efficiency of only 0.25 seconds per dataset, which makes it suitable in real-time applications. It is also highly applicable in practice, with programs such as the evaluation of wide-frequency fluctuations and energy efficiency optimization, which makes it very applicable to practical power electronics systems. Such strengths, along with its scalability, guarantee that the method is reliably and efficiently used in all sorts of power electronics applications.

The practical applicability of the proposed method in real-life situations is one of the main strengths. It is especially appropriate to complement such programs as wide-frequency fluctuation assessment and energy efficiency improvement. The method is a sound solution in power electronics systems, where the signals commonly vary across a wide range of frequencies, and where energy efficiency is a key issue. It directly helps to improve the performance of a system and minimize the energy losses by estimating the signal parameters correctly, minimizing the interference, and considering dynamic changes. This renders the approach very pertinent to enhancing the dependability and productivity of power electronics systems, including the ones employed in voltage control, reactive power compensation, and smart grid control.

6. CONCLUSION

Power quality issues may have their signal properties uncovered by using various signal processing methods. The length of the disruptions determines the sort of signals created, which in turn exhibit changes in both frequency and amplitude. High junction temperatures in switching devices are often a result of improved converter topologies designed to meet high-power and high-efficiency

system requirements. Power electronic circuit designers might attempt to reduce reliability difficulties by learning how the electrical and thermal properties of the semiconductor devices used in the circuit interact with one another. Pulsed currents are the norm for power electronic systems. When designing dependable power electronics systems, it is not practical to think about the continuous rating of semiconductor components. In order to keep system reliable, power electronic systems must be carefully designed.The first three of these potential mistake causes have already been covered in this work. Power electronic circuits' ability to process energy accurately is very sensitive to the causes of digital control circuit errors. Fixing these mistakes increases the separation of the signal and noise/distortion parts, which in turn improves the input/output voltage and current parameters. It is worth mentioning that in many cases, the only way to make improvement is to alter the algorithms rather than the hardware.

To prevent the aliasing phenomena from severely degrading the signal properties during the digital-to-analog signal conversion process, the sampling speed must be carefully chosen. It is critical to use simultaneous sampling for systems that have more than one analog input in order to sample signals simultaneously. Another critical factor in jitter elimination is the stability of the sampling pulses. This study demonstrates the issues that develop in multirate digital control circuits when the signal sampling rate is varied. Furthermore, techniques for mitigating quantization noise via the use of oversampling and noise-shaping circuits are shown.

In addition, the article introduces a novel method for determining the resulting signal-to-noise ratio in a three-stage digital control program. Power electronic control circuit designers may use this method to predict quantization errors and pick the right components.

Finally, the suggested approach has an outstanding level of accuracy, as evidenced by the low error rates, and resilience in harsh environments, including noise, frequency modulation, and dynamic changes. Its capability to effectively reduce interference and at the same time attain high accuracy in real world applications highlights its reliability. Also, the practical applicability of the method in the programs such as wide-frequency fluctuation evaluation and energy efficiency enhancement also underscores the importance of the method in the contemporary power electronics systems.

Problems in transforming analog circuitry into digital ones are also covered in the article.

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